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H. KNICKERBOCKER

Development of an Electronic Interface for a Fiber Optic Interferometric Sensor

W.H. Glenn,
H. Knickerbocker,
and A.P. Weise

May 1981

Prepared for the

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This report documents the design, fabrication, and testing of an electronic interface unit for a fiber optic interferometric sensor. The unit is a wide dynamic range, highly linear FM demodulator for the detection of low modulation index FM signals in the presence of large, low frequency interfering signals. Outputs to drive acousto-optic frequency shifters are provided. The report includes complete parts lists and schematic drawings for two units delivered to the sponsoring agency, Naval Research Laboratory.

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Development of an Electronic Interface For a Fiber Optic Interferometric Sensor

1. INTRODUCTION

The objective of this program was to design, fabricate, test and deliver to NRL, two electronic interface units for use with an interferometric fiber optic acoustic sensor.

The basic function of the interface unit is that of an FM receiver. It is capable of detecting modulation components of extremely low modulation index ($\sim 10^{-6}$ rad) at acoustic frequencies in the presence of interfering signals at low (< 10 Hz) frequencies but with large modulation indices. In addition, it provides appropriate signals to drive acousto-optic modulators for frequency shifting the signals in the two arms of an optical heterodyne interferometer.

The receiver uses a high stability, low phase noise 10 MHz oscillator as the primary frequency standard. A frequency synthesizer derives signals at 40 MHz and 40.5 MHz (or 39.5 MHz) from this oscillator. These are to be used to drive acousto-optic modulators to produce frequency offsets in each of the two arms of an optical heterodyne interferometer. Frequency offsets are provided for both arms to allow freedom of choice of the difference frequency while maintaining the basic shift frequency near 40 MHz for convenient operation of Bragg cells.

In the frequency synthesizer, the 10 MHz frequency is doubled twice to produce a 40 MHz signal. The 10 MHz signal is also counted down by a factor of 20 to produce a 500 kHz signal, the basic if frequency. This signal is combined with the 40 MHz signal in a single sideband suppressed carrier modulator to produce a signal at 40.5 MHz (or 39.5 MHz, if desired).

Optical mixing of the signals from the two arms of the interferometer will give a beat frequency of 500 kHz. This will be phase (or frequency) modulated by the desired acoustic signal together with undesirable thermal drift signals. This signal is FM demodulated in a wide dynamic range, highly linear FM demodulator to produce the desired output signal.

In an FM demodulator, the requirements for adequate sensitivity and extreme linearity of the output voltage vs frequency characteristics are generally conflicting, and a compromise must be made. A transmission line bridge discriminator was chosen for its good linearity. This type of descriminator has an output voltage vs frequency characteristic that approximates a sawtooth or triangular wave. It can be used as a discriminator at any frequency corresponding to a zero crossing.

In the receiver, the 500 kHz signal is multiplied up to 4 MHz to increase the FM deviation. This signal is then applied to the bridge discriminator. Three discriminator characteristics are provided. These correspond to discriminators with first zero crossings at 800 kHz, 364 kHz and 190 kHz. These are operated at the 5th, 11th or 21st zero crossings to provide the discriminator characteristic at 4 MHz.

This open loop approach was selected over a variety of phase-locked loop and frequency feedback schemes involving voltage controlled oscillators (VCO) for two principal reasons: neither the phase stability nor the linearity of the frequency versus voltage characteristics of available VCO's appear adequate for the present application. Phase-locked loop techniques have been extensively developed for FM demodulation, and they can represent an optimum approach for the detection of high modulation index FM signals having a low carrier-to-noise ratio; i.e., near the FM threshold. The present application is the other extreme, with a very high carrier-to-noise and a very low modulation index. This imposes different constraints on the receiver design. Detailed discussions of the merits of various approaches are presented in UTRC Reports R79-924576-1 and R80-924576-2, prepared under Contract N00173-C-0421.

2. TRANSMISSION LINE BRIDGE DISCRIMINATOR

This section presents a brief description of the operation of the transmission line bridge discriminator. The basic configuration is shown in Fig. 1. The two upper arms are fixed resistors. The two lower arms consist respectively of an open and a shorted transmission line of equal lengths. The resistor values are chosen to be equal to the characteristic impedance of the transmission line ($\sim$ 50 ohms in practice). The signals from the two midpoints of the bridge are peak detected and the difference is taken to give the desired output signal. Standard transmission line formulas give for the impedance of an open line

$$\frac{Z}{Z_o} = j \tan \beta\ell$$

The voltage at the center of the open line branch (for unity amplitude input) is then

$$V_1 = \frac{Z_o \; j \tan \beta\ell}{R + j \, Z_o \tan \beta\ell} = \frac{j \tan \beta\ell}{1 + j \tan \beta\ell}$$

$$= \frac{j \sin \beta\ell}{\cos \beta\ell + j \sin \beta\ell} = j \, e^{-j\beta\ell} \sin \beta\ell$$

and the magnitude of this, detected by the peak detector, is simply

$$|V_1| = |\sin \beta\ell|$$

A similar calculation for the shorted line branch gives

$$|V_2| = |\cos \beta\ell|$$

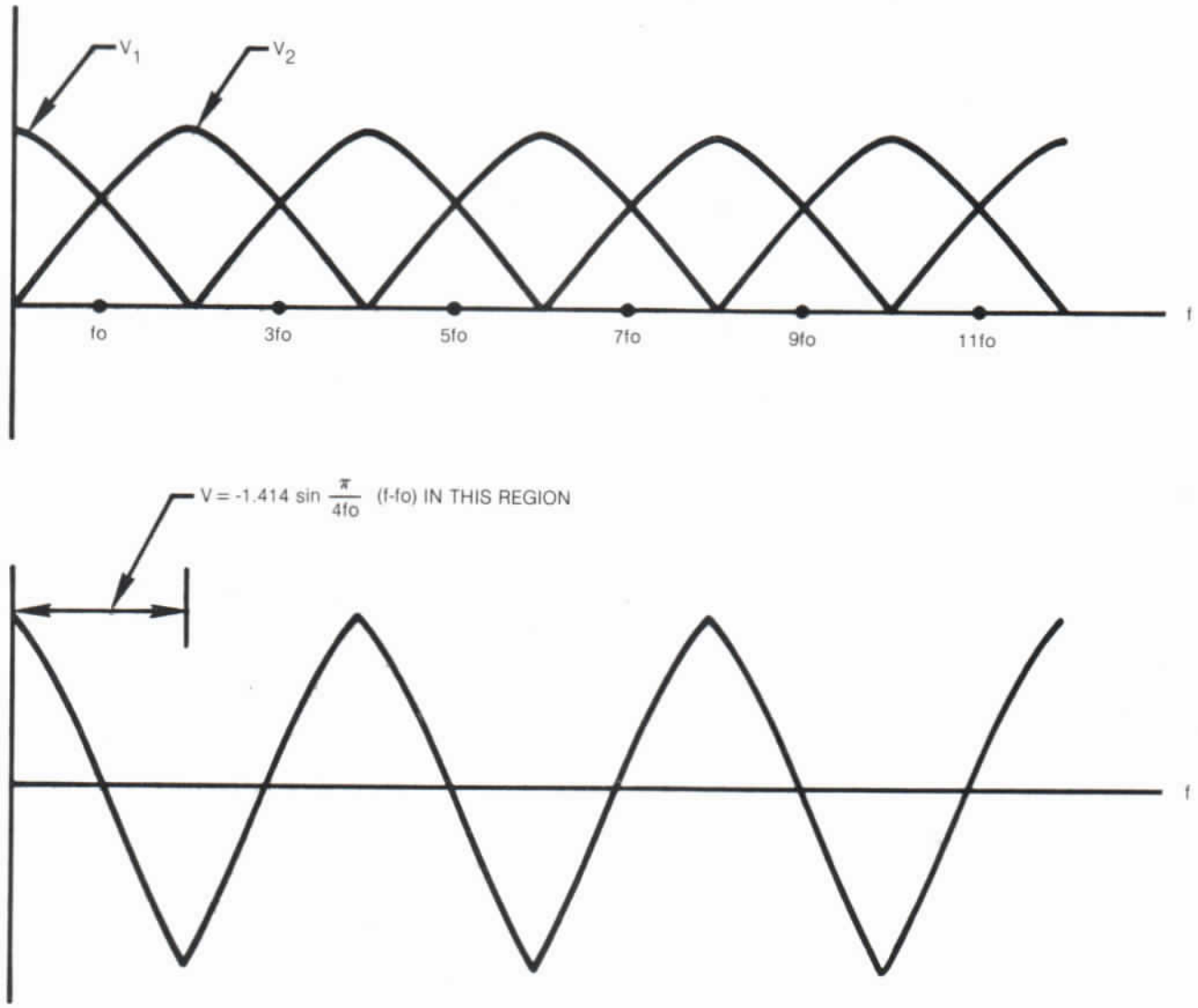
The output voltage is thus

$$V_o = |V_2| - |V_1| = |\cos \beta\ell| - |\sin \beta\ell|$$

and is zero if $\beta\ell$, the electrical length of the line, is any odd multiple of $\pi/4$ (45°). The output voltage vs frequency approximates a triangular wave as shown in Fig. 2. (Note $\beta\ell = 2\pi\ell/v \; f$, with v = propagation velocity.) The bridge may be used as a discriminator with a center frequency corresponding to any one of the zero crossings. Increased sensitivity can be achieved by making the period of the characteristic shorter (i.e., using longer delay lines). Wider range and

FIG. 1

DELAY LINE BRIDGE



fo = FREQUENCY FOR WHICH THE LINE IS λ/8

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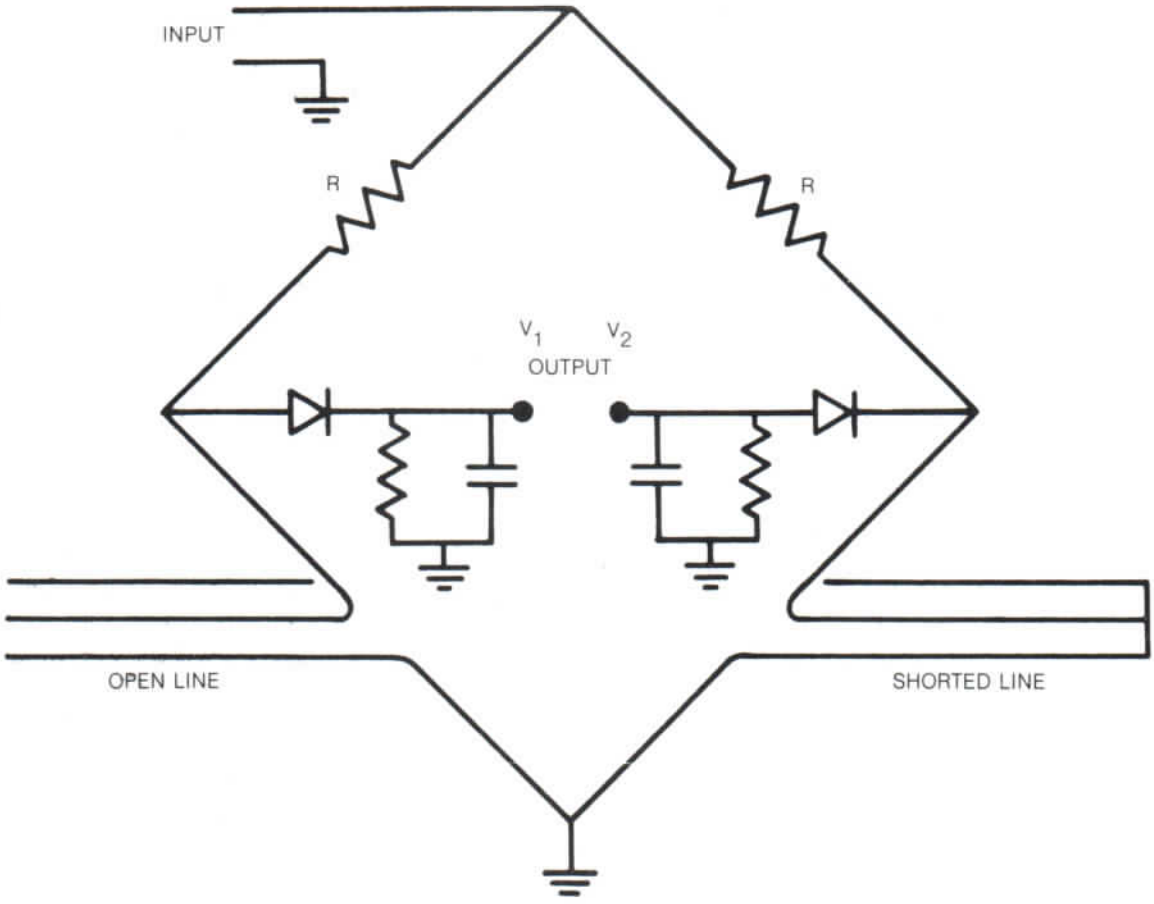
DELAY LINE BRIDGE



R = Zo FOR TRANSMISSION LINES

81-5-105-3

increased linearity results from making the period longer (i.e., using shorter delay lines). It is straightforward to show that within any of the quasi-linear segments, the characteristic is given by

$$V_o = \pm 1.414 \sin \frac{\pi}{4} \frac{\Delta f}{f_o}$$

where Δf is the frequency deviation from the zero crossing and f_o is the frequency of the 1st zero crossing. Using this expression, we may estimate the linearity ofthe discriminator. The characteristic may be expanded for small $\Delta f/f_o$ as

$$\sin \frac{\pi}{4} \frac{\Delta f}{f_o} \approx \frac{\pi}{4}\left(\frac{\Delta f}{f_o}\right) - \frac{1}{3!}\left(\frac{\pi}{4} \frac{\Delta f}{f_o}\right)^3 .$$

we now assume

$$\Delta f = F_o \sin \Omega t$$

The amplitude of the fundamental output will be

$$A_1 = \frac{\pi}{4} \frac{F_o}{f_o}$$

and that of the third harmonic will be

$$A_3 = -\frac{1}{4} \frac{1}{3!}\left(\frac{\pi}{4} \frac{F_o}{f_o}\right)^3 .$$

(here the relation $\sin^3 x = (3 \sin x = \sin 3x)/4$ was used.)

The ratio of the amplitudes of the third harmonic component to the fundamental is thus

$$|A_3/A_1| = (\pi F_o/4f_o)^2/24$$

Consider a disturbance of 100 radians at $\Omega = 2\pi \times 1$ Hz, i.e., $\Delta f = 100 \sin \Omega t$, $F_o = 100$. For the most linear mode of operation of the receiver, $f_o = 800$ kHz. For this case $(A_3/A_1) = 4 \times 10^{-10}$, or a power ratio of -194 dB. The amplitude $A_3 = 3.9 \times 10^{-14}$. This is the amplitude corresponding to an applied signal of 1.3×10^{-8} radians at 3 Hz. If the disturbance is increased to 1000 rad, A_3

increases by 10^3 and the corresponding minimum detectable signal at 3 Hz is 1.3×10^{-5} radians. Such a high degree of linearity could not be verified in practice due to the intrinsic harmonic content of conventional signal generators used to produce test signals.

3. DESCRIPTION OF RECEIVER

3.1 General

The receiver is constructed in four rack mountable 19 in. enclosures. It is shown in Fig. 3. This approach was taken to break the system into functional units which could be developed on a stand-alone basis. The four units are a dual 40 MHz signal generator, acoustic optical modulator driver/power supply, receiver, and discriminator timing cable assembly.

All circuitry is mounted in shielded, bypassed enclosures and interconnected with coaxial cables. Every possible component or assembly that could be purchased from vendors was acquired to keep development costs to a minimum. Circuitry fabricated at UTRC includes the countdown circuit in the 40 MHz signal generator and the limiter and discriminator in the receiver.

All circuitry is designed in a modular manner to allow flexibility in the design and testing of this system.

SPECIFICATIONS

General

AC Power - 1 amp at 110 Vac
Warm up - 15 minutes from cold start

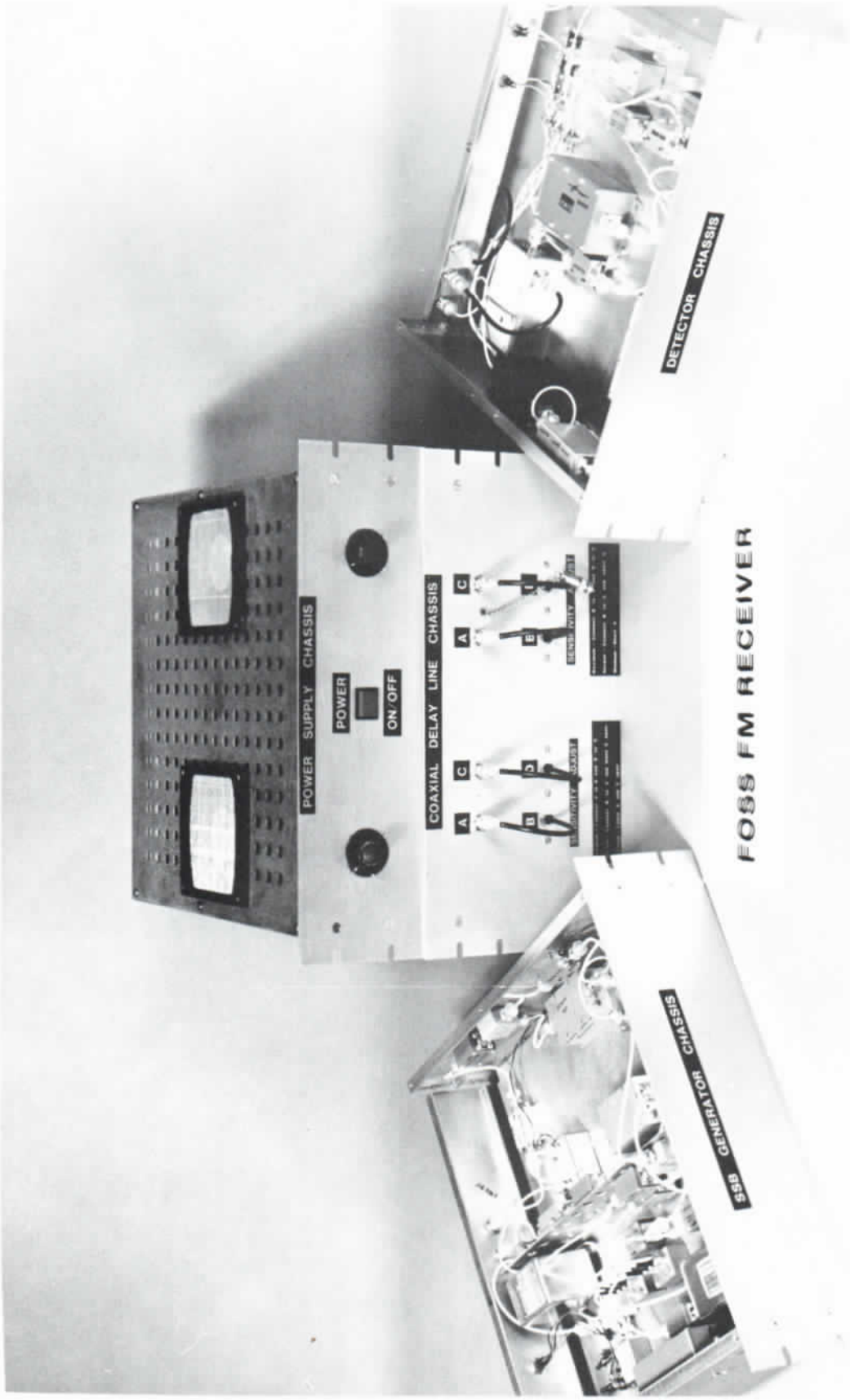
Acoustic Optical Modulator Driver

Output Frequencies: 40 and 40.5 MHz (39.5 MHz is user selectable)
Output Capability: +7 to +37 dBm into 50 Ω - Front panel adjustable
All spurious: > 20 dB below CARRIER

Receiver

Input Frequency: 500 kHz
Input Level: +4 dBm to +10 dBm into 50 ohms
Input Impedance: 50 ohms
Output Sensitivity: -38 dBv for 100 Hz deviation (1 radian at 100 Hz modulation frequency) or 0.25 mV/Hz
Output Noise Floor: -155 dBv in 1 Hz bandwidth or 17 $nV/(Hz)^{1/2}$
Minimum Detectable Signal: 1.4×10^{-6} radians at 100 Hz
Otuput Impedance (Nominal): 600 ohms
Output Bandwidth: 2-20,000 Hz

FIG. 3


FOSS FM RECEIVER
SSB GENERATOR CHASSIS
POWER SUPPLY CHASSIS
POWER
ON/OFF
COAXIAL DELAY LINE CHASSIS
A
C
A
C
DETECTOR CHASSIS

Linearity: Accurate linearity measurements below 0.1% were limited by available signal generators. No degradation was noted on modulated signals that had this distortion level at the input of the receiver. This held true for all modulation frequencies in the band of interest.

A complete drawing package is provided. Block diagrams are included for all the major assemblies and schematic diagrams are provided for all UTRC designed circuitry. A complete set of parts lists are included to allow acquisition of spare parts. The drawing package is listed on drawing number ESG 634-3-1.

There are two deviations from the original plan for the receiver. A preamplifier is required to interface a photodetector with the receiver input. The preamplifier must be matched to the detector that will be used. A best guess was made on this circuit, but the input impedance should be adjusted for best performance. No biasing provision for the detector is provided. Only one preamplifier has been supplied. A second unit can be supplied if desired. No filtering or amplification of the output signal from the receiver has been provided. All measurements were made with a spectrum analyzer. Selection of an amplifier and filter is dependent on the desired subsequent processing of the output signal.

There are several areas for further work on a second generation receiver. Cost and size could be reduced by using printed circuit-compatible components. The use of miniature delay lines to replace the coaxial cable networks should be investigated. The precision oscillator is one of the most expensive components in the system ($\sim$ \$1000). Preliminary tests with a TTL output, temperature compensated oscillator (VECTRON CO-231-T) showed marginally acceptable results. These units are less expensive ($\sim$ \$100) and should be investigated.

3.2 Receiver Chassis

The receiver section of the system operates at an input frequency of 500 khz and a nominal input level of +4 dBm into 50 ohms. The construction is modular to allow rapid implementation of design changes and analysis of individual circuit functions. The block diagram of the circuit is drawing number ESG 634-1-1.

The input signal is doubled in frequency three times, to 4 MHz. This deviation multiplier increases the sensitivity of the receiver. The selection of intermediate frequency, and number of multiples was chosen as the best compromise with the required length of timing cable needed in the discriminator. The 4 MHz signal is passed through a band-pass filter (BPF-1) to set the bandwidth of the system. This is a one-pole series L-C section with a -3 dB bandwidth of 100 kHz.

The signal is hard limited by the amplitude limiter to remove any amplitude fluctuations. This circuit is described in detail in the text. The signal is amplified to approximately +28 dBm and then applied to the discriminator which is also described in detail.

Regulated dc power is provided by three-pin monolithic regulators mounted at the chassis. The schematics and the component values for the various low pass and band-pass filters are described on drawing number ESG 634-1-2.

No effort was made to miniaturize this chassis or any other segment of the system. All of the components used in the low level signal processing are available in printed circuit board mounting varieties. The entire system could certainly be manufactured in one chassis with the implementation of this technique and the replacement of the timing cables with LC delay lines.

3.3 Single Side Band Generator

This subsystem synthesizes two signal in the 40 MHz region from one common low phase noise 10 MHz oscillator. Thise signals are the drive sources, after amplification, for the acoustic optical modulators. The difference frequency of these two signals is the input frequency for the receiver subsystem. The block diagram for this unit is ESG 634-1-3.

A 40 MHz signal is generated by frequency doubling twice the 10 MHz reference frequency. The signal at plus or minus the reciever frequency (39.5 or 40.5 MHz) is generated by a phasing type single side band generator. The 10 MHz reference is counted down to 500 kHz by the divide by 20 logic circuit. This circuit is more fully described elsewhere in the text. This 500 kHz signal is divided in quadrature and applied to two doubly balanced mixers driven by the 40 MHz channel. The outputs of these two mixers, which contain both 39.5 and 40.5 MHz energy, are summed into a second quadrature hybrid where, depending on the phasing selected, one of the side bands is effectively cancelled and the other is enhanced by +3 dB.

Great care was taken to maintain amplitude and phase balance in this circuitry. Carrier suppression was -30 dB, and opposite side band suppression was -37 dB in one unit and -46 dB in the other. Other spurious were -25 dB or better, except for 38.5 MHz energy at about -20 dB in both units.

The effect of spurious signals upon the capabilities of the system are unknown, since an optical test bed was not available for system evaluation. If further suppression is needed, filtering can be added at the output of the two mixers or at the output of the summing quadrature hybrid. The latter point is preferred since the filter would not introduce phase shifts into the SSB generator at this point.

3.4 Driver/Power Supply Chassis

This chassis contains both the dc power supplies for the system and the high power driver amplifiers for the optical modulators. The unit is powered from a 110 Vac 60 Hz single phase service. This service is fused and passed through a RFI line filter before being applied to the system power supplies.

Two regulated power supplies are mounted in this chassis. The first is a 5.5 amp, 24 Vdc unit which is required for the high power amplifiers, oscillator oven heater and as a source for various three-pin voltage regulators mounted in the other units to provide +15, +12, and +5 Vdc on a local basis. The second supply is a modulator, lower power unit that provides a negative 5 Vdc bias for the limiter units in the receiver chassis.

The two optical modulator driver amplifiers are Amplica model number 500 VSP. They are capable of +37 dBm output at -1 dB of amplitude compression and have a fixed gain of +38 dBm. Variable attenuators are provided on the front panel of the unit. These 0-30 dB attenuators allow the output level to be set from +7 dBm to +37 dBm. A fan is mounted directly above each amplifier to insure stable thermal behavior of the amplifier, since each of these class A units dissipates approximately 30 watts.

Rear panel connectors and interconnecting cables are provided to distribute dc power to the synthesizer and receiver decks. A front panel switch and indicator provides a means of switching and monitoring the ac input power. This is the only chassis that contains lethal voltages. For this reason, care should be taken when trouble shotting this unit with the protective cover removed.

The schematic drawing for this chassis and the power interconnect is ESG 634-1-4.

3.5 Limiter/Amplifier

A high speed comparitor (> 50 MHz) was chosen for the limiter function in this receiver. The 4 MHz signal level is well defined, therefore, dynamic range is not the major consideration. A well-defined (TTC logic level) output is more important to reduce spurious effects due to AM leakage into the detector circuitry.

The comparitor is connected in the zero crossing detection mode and is driven at approximately +7 dBm. The circuit is well decoupled and uses ground plane printed wiring techniques to reduce spurious effects due to power supply variation.

The output of the comparitor is fed to the same precision TTL to sine wave converter circuit used in the count down circuit. Additional buffering is provided by the R8, 9 and 10 passive attenuator. The schematic drawing for this circuit is ESG 634-1-5.

3.6 Count Down Circuit

The count down circuitry takes the precision 10 MHz signal from the crystal oscillator, makes it TTL compatible, counts it down to the desired intermediate frequency and then actively filters it to a sine wave.

Transistor Q1 and its associated circuitry comprise a low noise sine wave to TTL logic level converter.

IC-1 and IC-2 are TTL counters. The signal from the collector of Q1 is applied to the appropriate input as determined by the truth table on the schematic drawing. Wire jumpers are provided for on the board to select any one of the six intermediate frequencies between 0.1 and 5.0 MHz.

The output of the count down is applied to the transistor pair Q2 and Q3. This circuitry is a square wave to sine wave converter. Additional low pass filtering is provided by the L1 and C1 combination.

Regulated power for the circuit is produced by three-pin regulators IC3 and IC4 from the +24 Vdc bus. This circuitry was described in a Hewlett Packard Application Note #301-1. It is recommended for use with the precision, low-noise oscillator selected for this system. The schematic drawing pertaining to this circuitry is ESG 634-1-6.

3.7 FM Discriminator

The discriminator is a bridge type design employing coaxial cable as the resonant elements. The detector is driven at approximately +30 dBm and the signal is resistively split into the two legs of the bridge network. The coaxial cable is cut at an odd integer multiple of 45° of electrical length at the 4 MHz input frequency. Various lengths of cable are included to provide recovered signal versus linearity tradeoffs. The mechanical and electrical details of these coaxial assemblies are described in the section of this text pertaining to the timing cable chassis.

The sine and cosine timing functions provided by the open and shorted cables are capacitively coupled to the peak detector network D1 through D4 by capacitors C1 and C2. The diode network functions as a voltage doubler and peak charges capacitors C3 and C4. Dc bias for the diode network is accomplished by resistor R5.

The recovered information in the audio spectrum is high pass filtered by capacitors C5 and C6. The signals are added across the R7, R8 and R9 resistor combination. R8 is a potentiometer which acts as a balance control and has the

capability of reducing error due to AM feedthrough. Inductor L1 and capacitor C7 form a low pass network to remove 4 MHz leakage from the output signal. Resistors R6 and R10 provide a discharge path for C5 and C6.

The -3 dB bandwidth of the detector is 2 Hz to 20 kHz. No effort was made to provide bandpass filtering at the required 100 Hz to 3 kHz bandwidth since all tests employed a spectrum analyzer on the output of the receiver.

Several types of discriminators were evaluated including LC bridge (several variations), constant pulsewidth digital, and phase-locked loop. All were lacking for this application due to noise or linearity deficiencies. One approach that bears further investigation is the use of lumped constant tapped delay lines in place of the coaxial lines. A cursory looked proved this approach worked and would reduce the volume of the receiver. This scheme was not implemented in the final version due to an unexplainable sensitivity to noise pickup in these networks.

The drawing pertaining to this circuit is ESG 634-1-7.

3.8 Timing Cable Chassis

This chassis is an integral part of the receiver subsystem. The timing cables for the discriminator, due to their bulk, are mounted separately. The schematic diagram for this assembly is ESG 634-1-8.

Three sets of timing cables are provided to evaluate the sensitivity versus linearity tradeoff of various lengths of timing cables. The cables are cut to provide 45 degrees of electrical phase shift at 800, 364, and 190 kHz, depending on the cable length selected. The cable lengths are approximately 105, 225, and 430 feet per side, respectively.

The phase shift at 4 MHz is 225 degrees at the 800 kHz fundamental, 495 degrees at the 364 kHz fundamental, and 945 degrees at the 190 kHz fundamental. The 4 MHz signal is detected at the 5th, 11th or 21st zero crossing, depending on the cable selected.

The cables were cut to length using a stable 4 MHz reference and vector voltmeter. Irregularities in the velocity factor in the cable and some apparent dispersion at the lower frequencies make the 4 MHz measurement necessary. The length of the cables is critical to discriminator balance and linearity. The interconnecting coaxial cables between the receiver and timing cable chassis are part of the overall delay and, therefore, critical. These cables are supplied.

A possible replacement for these cables are LC delay lines. A cursory look was made at this approach, but noise sensitivity problems in our test setup mandated the use of coaxial cable. Certainly, if time and money permit, a further investigation of these devices would be warranted.

Instructions are provided on the front panel of this chassis as to the proper selection of the various sensitivity cables. The open and shorted terminations are also provided. The "A" cable is the least sensitive, and the "C" cable is the most sensitive.

3.9 Receiver Preamp

A receiver preamp has been constructed to provide an interface between the optical detectors and the receiver subsystem.

The circuit employs an integrated circuit differential high frequency amplifier (MC 1733) set at a gain of 10. The input impedance at both parts is 50 ohms to facilitate testing. Resistors R1 and R2 can be changed to match the impedance of the detectors.

The gain of the device can be changed to any value from 10 to 400. The specification sheet should be consulted to make a modification to the circuitry.

An emitter follower, Q1, was inserted to allow driving lengths of 50 Ω cable. This unit has not been tested with an optical system and is provided only on a best guess basis. The schematic drawing of this unit is ESG 634-1-8.

DRAWING LIST 1 OF 1						CHANGES	
UNLESS OTHERWISE SPECIFIED: CAPACITORS=500wvdc RESISTORS=CARBON. . . W ± . . . %, C-1=μμF, C-1=μF R=OHMS, L=μh ALL SYMBOLS – ASME, IEEE				APPRV. . . . . ORIG. . . . . CHK. . . . . DRAWN. . . . . DATE 5/15/81	TITLE – FOSS –	CHANGE DRAWN CHK. DATE	DISTR.
SCALE	MATERIAL	FINISH	TOLERANCES		UNITED TECHNOLOGIES RESEARCH CENTER		DRAWING NO. ESG 634-3-1 REV.

ESG
634

– 1-1	Receiver
– 1-2	Low Pass and Bandpass Filters
– 1-3	SSB Generator
– 1-4	Power Supply Chassis
– 1-5	Limiter
– 1-6	Count Down CKT
– 1-7	Discriminator
– 1-8	Timing Cable Chassis
– 1-9	Differential Preamp
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PARTS LIST

CHANGES

UNLESS OTHERWISE SPECIFIED CAPACITORS-500 wvdc			APPRV	TITLE	CHANGE	DISTR	
RESISTORS-CARBON W± %,C<1 µF			ORIG	Receiver Chassis (FOSS)	DRAWN		
R-OHMS,L-µh ALL SYMBOLS ASME-IEEE			CHK	UNITED TECHNOLOGIES RESEARCH CENTER	CHK	DRAWING NO	REV.
SCALE	MATERIAL	FINISH	TOLERANCES	DRAWN ..... DATE 3/19/81	DATE	ESG634-2-1	

CK.	QUAN	ITEM	DESCRIPTION	MANUFACTURE	IDENT. NO.
	1		680 kHz L.P.F	UTRC	
	3	GK-3	Frequency Doubler	Mini CKTS	
	2	UTO 502	R. F. Amplifier	AVANTEK	
	2	UTO 533	R. F. Amplifier	AVANTEK	
	1		1.1 MHz L.P.F. 5 Pole	UTRC	
	1		2.8 MHz L.P.F. 3 Pole	UTRC	
	1		Limiter	UTRC	
	1		4 MHz 1 MHz Wide B.P.F.	UTRC	
	1	ZHL-3A	R.F. Power Amplifier	Mini CKTS	
	1		Bridge Discriminator	UTRC	
	1		4 MHz B.P.F.	UTRC	
	4	UG492 A/V	BNC Bulk Head COnnector	AMPHENOL	056008
	2	126-218	5 Pin Female Connector	AMPHENOL	056100
	34	2331350-4	BNC Connector	AMP	056469
	1	UG914 A/V	Double BNC Female Adapter	AMPHENOL	056068
	1	7815	Voltage Regulator 15 Volt	Fairchild	
	1	7812	Voltage Regulator 12 Volt	Fairchild	
	1	7805	Voltage Regulator 5 Volt	Fairchild	
	1	4.7/35 V	Tantalum Capacitor	Mallory	057332
	3	1.0/50 V	Mono Capacitor	Erie	057329
	1	0.1/50 V	Mono Capacitor	Erie	057327
	1		Bottom Panel	Ventrak	067176

PARTS LIST

CHANGES

UNLESS OTHERWISE SPECIFIED CAPACITORS 500 w/dc
RESISTORS CARBON W ± %,C<1 μF
R OHMS,L μh ALL SYMBOLS ASME/IEEE

SCALE	MATERIAL	FINISH	TOLERANCES

APPRV .....
ORIG .....
CHK .....
DRAWN .....
DATE 3/19/81

TITLE
Receiver Chassis (FOSS)

UNITED TECHNOLOGIES RESEARCH CENTER

CHANGE
DRAWN
CHK
DATE

DISTR

DRAWING NO
ESG634-2-1

REV.

CK	QUAN	ITEM	DESCRIPTION	MANUFACTURE	IDENT NO.
	1		Front Panel	Ventrak	067171
	2		Side Panel	Ventrak	067162
	1		Back	Ventrak	067167
	1		Top Cover	Ventrak	067169

PARTS LIST

CHANGES

UNLESS OTHERWISE SPECIFIED CAPACITORS 500 wvdc
RESISTORS CARBON W ± %,C<1 μF
R-OHMS,L μh ALL SYMBOLS ASME/IEEE

SCALE	MATERIAL	FINISH	TOLERANCE %

APPRV .....
ORIG .....
CHK .....
DRAWN .....
DATE 3/19/81

TITLE
SSB GENERATOR (FOSS)

UNITED TECHNOLOGIES RESEARCH CENTER

CHANGE
DRAWN
CHK
DATE

DISTR

DRAWING NO
ESG634-2-3

REV

CK.	QUAN	ITEM	DESCRIPTION	MANUFACTURE	IDENT NO.
	2	UTO533	Amplifier	AVANTEK	
	3	UTO502	Amplifier	AVANTEK	
	8		3 dB Attenuator	UTRC	
	2	GK-3	Frequency Doubler	Mini CKTS	
	3	7FSC2-6	Power Splitter/Combiner 0°	Mini CKTS	
	1	7SCQ-2-50	Power Splitter/Combiner 90°	Mini CKTS	
	1	QH-7-4.9	Quadrature Hybrid	Merrimac	
	2	7LW-1-1	Mixer	Mini CKTS	
	1		÷ 20 Countdown	UTRC	
	1	10811 A	10 MHz Crystal Oscillator	HP	
	1		UA7815 Regulator 15 Volt	Fairchild	
	1		UA7812 Regulator 12 Volt	Fairchild	
	44	2-331350-4	BNC Connector	AMP	
	2	UG492 A/V	BMC Bulkhead	AMPHENOL	056469
	6	2031-5006-00 OSM511-3	OSM Connector	OMNI Spectra	056560
	1		50 OHM Termination	Pomona Electronics	
	1	UG1094/U	BNC Chassis Female UG-1094/U	AMPHENOL	056076
	1	126-218	5 Pin Female Connector	AMPHENOL	056100
	1		40 MHz 10 MHz Wide Bandpass FIlter	UTRC	
	1		20 MHz 4 Wide Bandpass Filter	UTRC	
	1	250 15 30 210	P.C.B. Connector	CINCH	
	1		7 dB Attenuator	UTRC	

PARTS LIST

CHANGES

UNLESS OTHERWISE SPECIFIED CAPACITORS 500 wvdc
RESISTORS CARBON W± %,C<1 μF
R OHMS,L μh ALL SYMBOLS ASME/IEEE

SCALE	MATERIAL	FINISH	TOLERANCES

APPRV .....
ORIG .....
CHK .....
DRAWN .....
DATE 3/19/81

TITLE
SSB Generator (FOSS)

UNITED TECHNOLOGIES RESEARCH CENTER

CHANGE
DRAWN
CHK
DATE

DISTR

DRAWING NO ESG634-2-3

REV.

CK.	QUAN	ITEM	DESCRIPTION	MANUFACTURE	IDENT. NO.
	2	4.7/35 V	Tantalum Capacitor	Mallory	057332
	2	1.0/50 V	Mono Capacitor	Erie	057329
	1	0.1/50 V	Mono Capacitor	Erie	057327
	1		Bottom Panel	Ventrak	067176
	1		Front Panel	Ventrak	067171
	2		Side Panel	Ventrak	067162
	1		Back	Ventrak	067167
	1		Top Cover	Ventrak	067169

PARTS LIST

CHANGES

UNLESS OTHERWISE SPECIFIED CAPACITORS 500 wvdc
RESISTORS CARBON W ± %,C<1 μF
R OHMS,L μh ALL SYMBOLS ASME/IEEE

SCALE | MATERIAL | FINISH | TOLERANCES

APPRV .....
ORIG .....
CHK .....
DRAWN .....
DATE 3/19/81

TITLE
Power Supply Chassis (FOSS)

UNITED TECHNOLOGIES RESEARCH CENTER

CHANGE | DRAWN | CHK | DATE

DISTR

DRAWING NO ESG634-2-4

REV.

CK	QUAN	ITEM	DESCRIPTION	MANUFACTURE	IDENT. NO.
	2		0-30 dB Attenuator		
	1	513-1501-604	Switch	DIALCO	077055
	1	532-0901	Rectangular Bezel	DIALCO	077053
	1	303-3472	Lens	DIALCO	
	1	10B1	Line Filter	CORCOM	
		VA24MT550	24 Volt Power Supply	ACOPIAN	
		P1.5-1000	5 Volt Power Supply	SEMICONDUCTOR	CKTS 087046
	1	17408-P	Line Cord	Crib	058008
	1	SR-6P3-4	Cord Grip	HEYCO	058014
	2	HKP	Fuse Holder	BUSS	053182
	4	UG492 A/V	BNC Bulkhead Connector	AMPHENOL	056008
	2	126-218	5 Pin Female Connector	AMPHENOL	056100
	2	MOL-2	2 AMP Fuse (Slow Blow)	BUSS	
	1	5700A	Power Supply Socket	SEMICONDUCTOR	CKTS 085163
	2	500 VSP	R.F. Amplifiers	AMPLICA	
	4	2031-5006-00 OSM 511-3	OSM Connector	OMNI Spectra	056560
	2	BS2107FL	Fans	IMC MAGNETICS CORP	063010
	4	2-331350-4	BNC Connector	AMP	056469
	1		Bottom Panel	VENTRAK	067176
	1		Front Panel	VENTRAK	067171
	2		Side Panel	VENTRAK	067162
	1		Back	VENTRAK	067167

PARTS LIST

CHANGES

UNLESS OTHERWISE SPECIFIED CAPACITORS=500 wvdc	APPRV	TITLE: Power Supply Chassis (FOSS)	CHANGE
RESISTORS-CARBON, W±__%, C<1 μF	ORIG		DRAWN
R-OHMS, L-μh ALL SYMBOLS ASME/IEEE	CHK	UNITED TECHNOLOGIES RESEARCH CENTER	CHK
SCALE / MATERIAL / FINISH / TOLERANCES	DRAWN ..... DATE 3/19/81		DATE

DISTR.

DRAWING NO. ESG634-2-4

REV.

CK.	QUAN.	ITEM	DESCRIPTION	MANUFACTURE	IDENT. NO.
	1		Top Cover	VENTRAK	067169

PARTS LIST

CHANGES

UNLESS OTHERWISE SPECIFIED CAPACITORS-500 wvdc
RESISTORS CARBON W± %,C<1 μF
R-OHMS,L-μh ALL SYMBOLS ASME/IEEE

SCALE	MATERIAL	FINISH	TOLERANCES

APPRV .....
ORIG .....
CHK .....
DRAWN .....
DATE 3/19/81

TITLE
LIMITER (FOSS)

UNITED TECHNOLOGIES RESEARCH CENTER

CHANGE
DRAWN
CHK
DATE

DISTR

DRAWING NO ESG634-2-5

REV.

CK	QUAN	ITEM	DESCRIPTION	MANUFACTURE	IDENT. NO.
	8	C1,2,4,6,7,8	0.1/50 V Mono Capacitor	ERIE	
		12,13			
	3	C3,5,9	15/25 V Tantalum Capacitor	MALLORY	
	1	C10	5-50 pf Variable Capacitor		
	1	C11	240 pf 500V Mica Capacitor		
	1	R1	49.9 Ω 1% RN55 Resistor	MEPCO	
	2	R2,6	1K Ω 1% RN55 Resistor	MEPCO	
	1	R3	150 Ω 1% RN55 Resistor	MEPCO	
	1	R4	215 Ω 1% RN55 Resistor	MEPCO	
	1	R5	464 Ω 1% RN55 Resistor	MEPCO	
	1	R7	68.1 Ω 1% RN55 Resistor	MEPCO	
	2	R8,10	97.6 Ω 1% RN55 Resistor	MEPCO	
	1	R9	69.8 Ω 1% RN55 Resistor	MEPCO	
	2	L1, 2	10 μ hy Inductor	DELEVAN	
	1	IC1	NE521 Integrated Circuit	SIGNETICS	
	2	Q1,2	2N3906 Transistor	NATIONAL	086030
	1		2906 Pomona Box	POMONA	
	2		2451 BNC Connector	POMONA	

PARTS LIST

CHANGES

UNLESS OTHERWISE SPECIFIED CAPACITORS 500 wvdc
RESISTORS CARBON W ± %,C<1 µF
R OHMS,L µh ALL SYMBOLS ASME/IEEE

SCALE	MATERIAL	FINISH	TOLERANCES

APPRV .....
ORIG .....
CHK .....
DRAWN HC.....
DATE 11-80.....

TITLE
FOSS RCUR-COUNT DOWN

UNITED TECHNOLOGIES RESEARCH CENTER

CHANGE
DRAWN
CHK
DATE 3/19/81

DISTR

DRAWING NO ESG634-2-6

REV.

CK.	QUAN	ITEM	DESCRIPTION	MANUFACTURE	IDENT. NO.
		C1	Selected Silver Mica or Mono		----
		C2	.01 Mono CAP	CENTRALAB	CW 15C 103K
		C3-11	.1 Mono CAP	CENTRALAB	CW 15C 104K
		C12-15	15 µF D 250 Tantalum CAP	Crib	057334
		D1	Schottky Diode HSCH 1001	HP	IN6263
		IC1,2	74LS290 TTL ÷ 10	-	
		IC3,4	78M05 3 Pin, 500CT Regulator	Fairchild	
		Q1-3	ZN3906 Transistor	Crib	086030
		R1-4	215 Ω RN55 Metal Film	MEPCO	
		R5	909 Ω RN55 Metal Film	MEPCO	
		R6-8	1K Ω RN55 Metal Film	MEPCO	
		R9	464 Ω RN55 Metal Film	MEPCO	
		R10	68.1 Ω RN55 Metal Film	MEPCO	
		R11	2K 10T Pot	Beckman	66WR2K
		L1	Selected Mini Molded Inductor	DELVAN	

PARTS LIST

CHANGES

UNLESS OTHERWISE SPECIFIED CAPACITORS-500 wvdc
RESISTORS-CARBON W± %,C<1 μF
R-OHMS,L-μh ALL SYMBOLS ASME/IEEE

SCALE	MATERIAL	FINISH	TOLERANCES

APPRV .....
ORIG .....
CHK .....
DRAWN .....
DATE 3/19/81

TITLE: DISCRIMINATOR (FOSS)

UNITED TECHNOLOGIES RESEARCH CENTER

CHANGE
DRAWN
CHK
DATE

DISTR.

DRAWING NO. ESG634-2-7

REV.

CK	QUAN	ITEM	DESCRIPTION	MANUFACTURE	IDENT. NO.
	4	R1,2,3,4	110 Ω 1/2 W 5% Carbon Resistor		
	1	R5	49.9 K RN55 1% Resistor	MEPCO	
	2	R6,10	4.02 K RN55 1% Resistor	MEPCO	
	2	R7,9	402 Ω RN55 1% Resistor	MEPCO	
	1	R8	500 Ω POT	Beckman	91WR
	2	C1,2,7	.005 Disc Ceramic Capacitor	Sprague	057210
	2	C3,4	.0022 Disc Ceramic Capacitor	Sprague	057266
	2	C5,6	500/25V Electrolytic Capacitor		
	4	D1,2,3,4	HSCH 1001 IN6263 Diode	H.P.	
	1	L1	50 μ hy Inductor	DELEVAN	
	1		2906 Pomona Box	Pomona	
	4		2451 BNC Connector	Pomona	

PARTS LIST

CHANGES

UNLESS OTHERWISE SPECIFIED CAPACITORS-500 wvdc
RESISTORS CARBON W± %,C<1 μF
R-OHMS,L-μh ALL SYMBOLS ASME/IEEE

SCALE	MATERIAL	FINISH	TOLERANCES

APPRV .....
ORIG .....
CHK .....
DRAWN R.Bosse
DATE 3/15/81

TITLE
Timing Cable Chassis - FOSS

UNITED TECHNOLOGIES RESEARCH CENTER

CHANGE
DRAWN
CHK
DATE

DISTR

DRAWING NO ESG634-2-8

REV.

CK	QUAN	ITEM	DESCRIPTION	MANUFACTURE	IDENT. NO.
	6	UG492 A/V	BNC Bulkhead Connector	AMPHENOL	056008
	10	2-329082-1	BNC Connector	AMP	056470
	24		1/2" x 7" Aluminum Rods	UTRC	
	1		Bottom Panel	Crib	067176
	1		Front Panel	Crib	078172
	2		Side Panel	Crib	067163
	1		Back	Crib	067167
	1		Top Cover	Crib	067169
	850'		RG58 A/V Coax Cable	Crib	108063

PARTS LIST

CHANGES

UNLESS OTHERWISE SPECIFIED CAPACITORS-500 wvdc
RESISTORS CARBON W.± %,C<1 μF
R-OHMS,L μh ALL SYMBOLS ASME/IEEE

SCALE	MATERIAL	FINISH	TOLERANCES

APPRV .....
ORIG .....
CHK .....
DRAWN .....
DATE 5/15/81

TITLE: Differential Preamp (FOSS)

UNITED TECHNOLOGIES RESEARCH CENTER

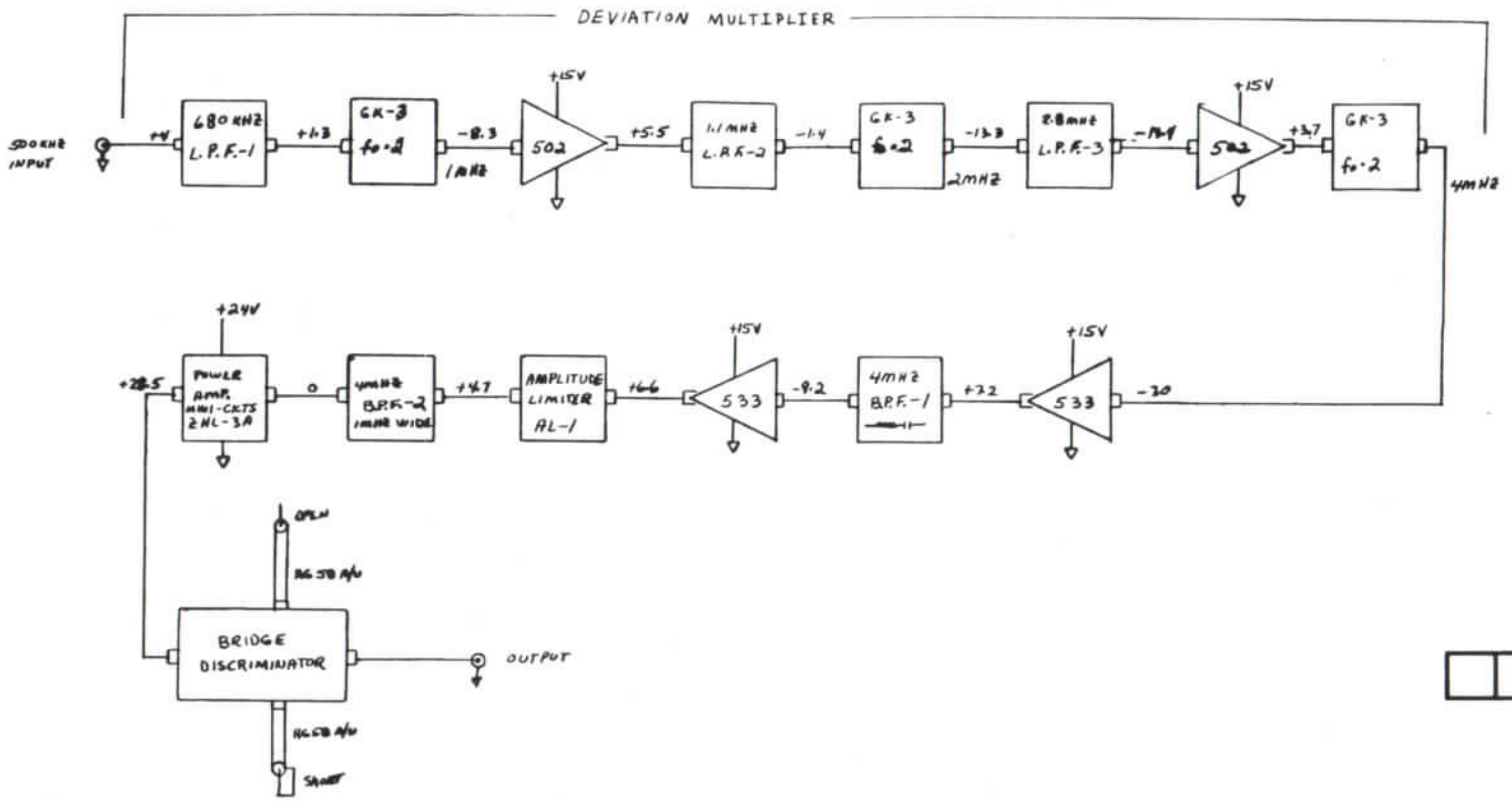
CHANGE
DRAWN
CHK
DATE

DISTR.

DRAWING NO. ESG634-2-9

REV.

CK.	QUAN	ITEM	DESCRIPTION	MANUFACTURE	IDENT. NO.
	2	B1, R2	49.9 Ω 1/4 W Metal Film Resistor	MEPCO	
	1	B3	1K 1/4 W 5% Carbon Resistor		
	2	R,4, R5	2K 1/4 W 5% Carbon Resistor		
	1	R6	100 Ω 1/4 W 5% Carbon Resistor		
	1	R7	33 Ω 1/4 W 5% Carbon Resistor		
	3	C1, C2, C11	.01/50 V Mono Cap	Erie	057326
	4	C3, C4, C5, C6	.1/50 V Mono Cap	Erie	057327
	1	C7	68 pF/500 V Ceraminc Disc	Sprague	
	2	C8, C10	1.0/50 V Mono Cap	Erie	057329
	1	C9	15/25 V Tantalum	Mallory	057334
	1	IC1	MC1733G	Motorola	
	1	Q1	2N5109	RCA	
	1		2906 Pomona Box	Pomona	
	3		2451 BNC Connector	Pomona	



ALL LEVELS MEASURED IN DBM
AMPLIFIERS ARE AVANTEK

UNITED TECHNOLOGIES RESEARCH CENTER

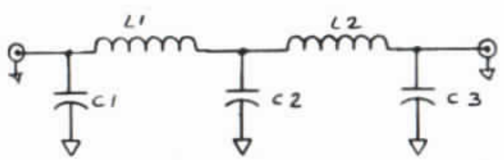
UNLESS OTHERWISE STATED
1. DIMENSIONS ARE IN INCHES
2. TOLERANCES ARE
± 0.08 FOR ONE DECIMAL
± 0.03 FOR TWO DECIMALS
± 0.01 FOR THREE DECIMALS
± 1° FOR ANGLES

RECEIVER — FOSS

PROJ. NO. 925266

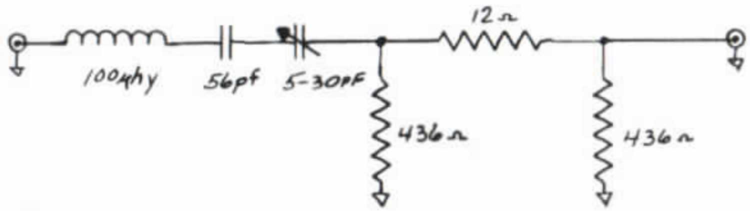
ESG634-1-1

LOW PASS

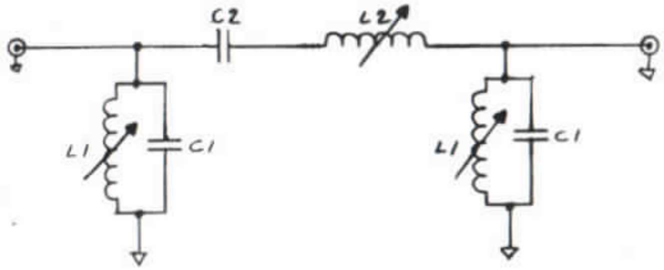


	C1	C2	C3	L1	L2
680 KHZ	6000pf	.01μf	6000pF	20μhy	20μhy
1.1 mHZ	.0033μf	.005μf	.0033μf	10μhy	10μhy
2.8 mHZ	.0015μf	.0015μf		4.7μhy	

4mHZ BANDPASS 100 KHZ WIDE



BAND PASS



	C1	C2	L1	L2
4mHZ 1mHZ WIDE	.0033 μf	100pF	.5μhy	15.9μhy
20mHZ 4mHZ WIDE	900pf	16pf	.08μhy	4μhy
40mHZ 10mHZ WIDE	318pf	10pf	.05μhy	1.6μhy

THESE CKTS ARE USED IN THE RECEIVER

INSPECTION REQ'D DIMENSIONS MARKED ● — TOTAL —	ENGINEER	LOW PASS AND BAND PASS FILTERS -FOSS- (RECEIVER)
UNLESS OTHERWISE STATED 1. DIMENSIONS ARE IN INCHES 2. TOLERANCES ARE ± 0.05 FOR ONE DECIMAL, ± 0.03 FOR TWO DECIMALS ± 0.01 FOR THREE DECIMALS ± 1° FOR ANGLES	WORK SHEET / PARTS LIST	
	ITEM / ZONE	MAT'L
PROJ. ENG. APN 5/81	NO. REQ'D	NEXT ASS'Y / PROJ. NO.
CH. OF DES.		
DES. SUP.		UNITED TECHNOLOGIES RESEARCH CENTER
DESIGNER	SCALE	East Hartford, Connecticut 06108
CHK. BY		UNITED TECHNOLOGIES
DRAWN BY R. Gasse 3/18/81		

REV.	BY	DATE	APP.

DWG. NO. 556634-1-2

REV

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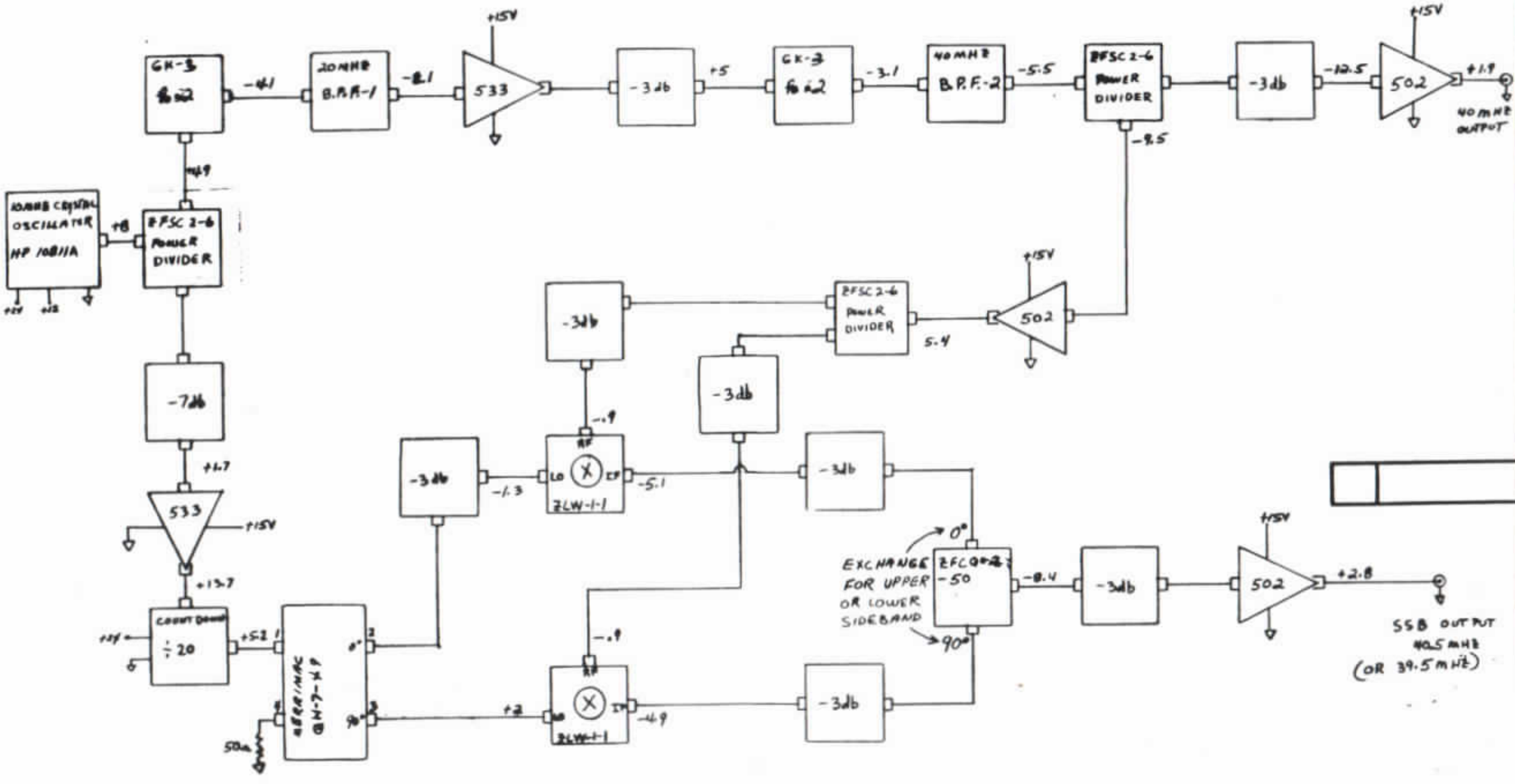


ALL LEVELS MEASURED IN DBM

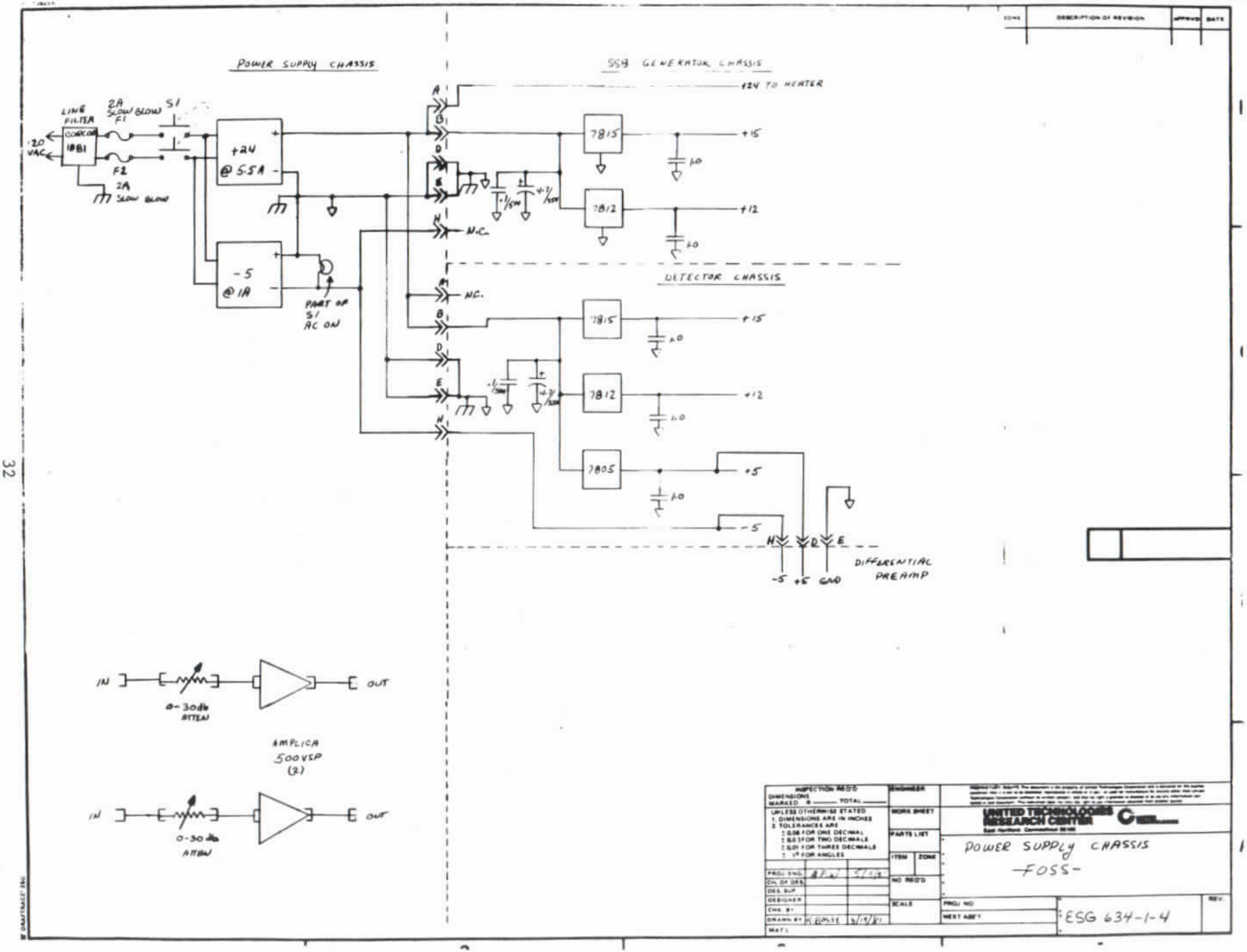
AMPLIFIERS ARE AVANTEK

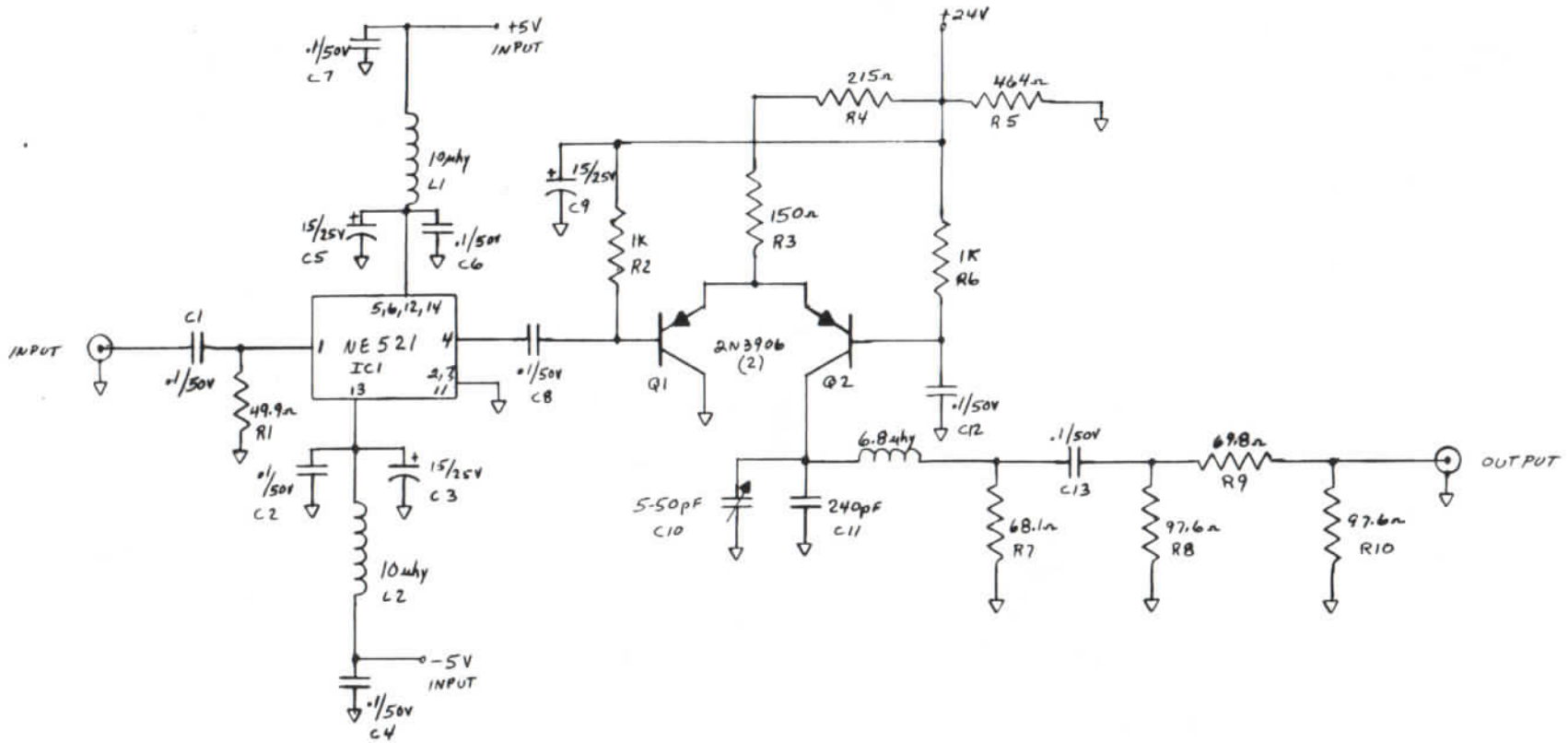
UNITED TECHNOLOGIES RESEARCH CENTER

East Hartford, Connecticut

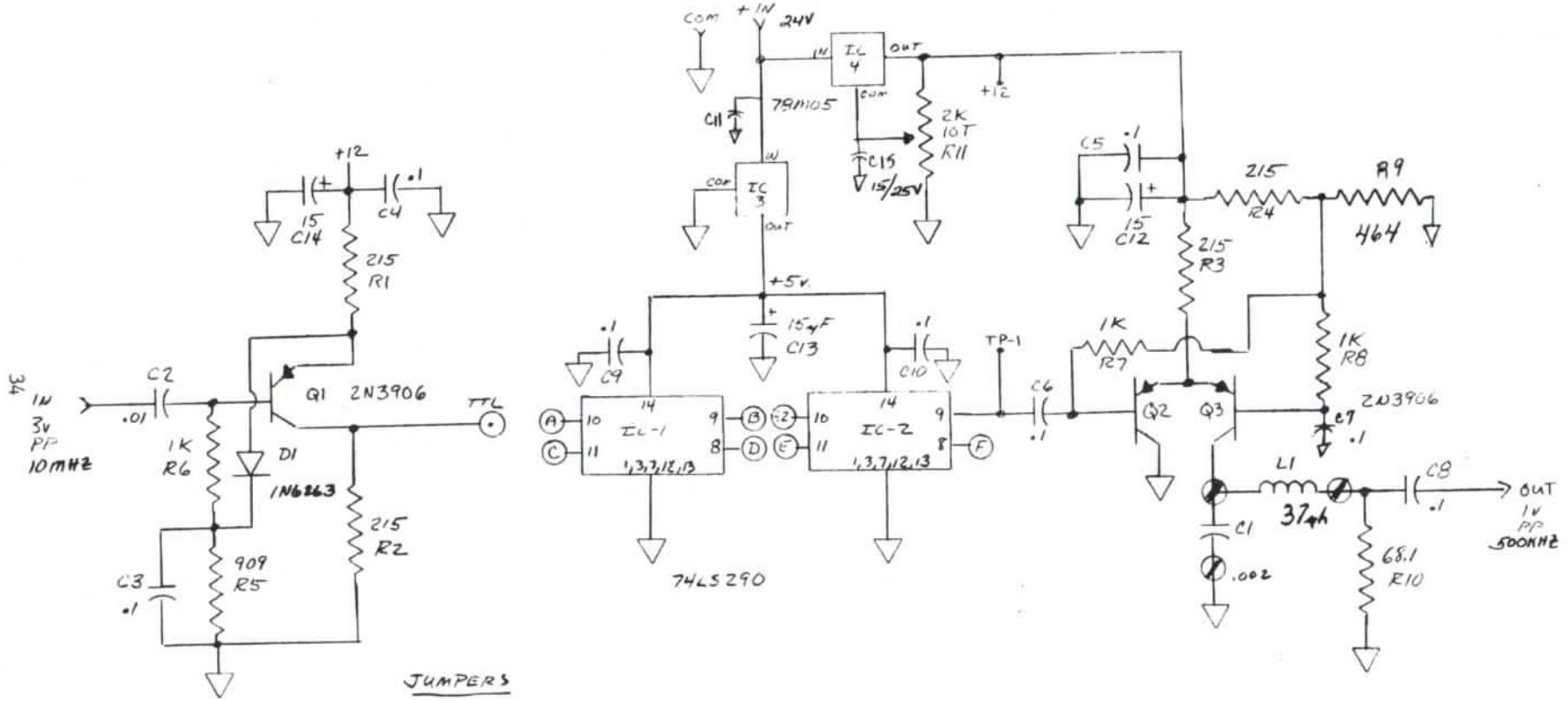
FOSS - SSB GENERATOR

ESG 634-1-3


POWER SUPPLY CHASSIS
SSB GENERATOR CHASSIS
DETECTOR CHASSIS
LINE FILTER
120 VAC
2A SLOW BLOW F1
F2 2A SLOW BLOW
S1
+24 @ 5.5A
-5 @ 1A
PART OF S1 AC ON
+24 TO HEATER
7815
7812
7805
+15
+12
+5
-5
N.C.
DIFFERENTIAL PREAMP
-5 +5 GND
IN
OUT
0-30db ATTEN
AMPLICA 500 VSP (2)
POWER SUPPLY CHASSIS -FOSS-
ESG 634-1-4



INSPECTION REQ'D DIMENSIONS MARKED ● ——— TOTAL ———	ENGINEER	LIMITER SCHEMATIC - FOSS - (PART OF RECEIVER)	REV.	BY	DATE	APP.	DWG. NO. 925264-5
UNLESS OTHERWISE STATED 1. DIMENSIONS ARE IN INCHES 2. TOLERANCES ARE ± 0.06 FOR ONE DECIMAL ± 0.03 FOR TWO DECIMALS ± 0.01 FOR THREE DECIMALS ± 1° FOR ANGLES	WORK SHEET						
	PARTS LIST						
	ITEM / ZONE	MAT'L					
		NEXT ASS'Y	PROJ. NO. 925265				
PROJ. ENG. J.P.K.	NO. REQ'D	PROPRIETARY NOTICE: This document is the property of United Technologies Corporation and is delivered on the express condition that it is not to be disclosed, reproduced in whole or in part, or used for manufacture for anyone other than United Technologies Corporation without its written consent, and that no right is granted to disclose or use any information contained in said document. This restriction does not limit the right to use information obtained from another source.					REV.
CH. OF DES.							
DES. SUP.							
DESIGNER	SCALE	UNITED TECHNOLOGIES RESEARCH CENTER East Hartford, Connecticut 06108					
CHK. BY							
DRAWN BY A. Bosse 3/19/81							



JUMPERS

FREQ MHz	TTL	÷2	OTHER
5	O	O	
2.5	A	B	
1	C	D	
.5	A	F	B-E
.2	C	F	D-E
.1	A	F	B-C D-E

INSPECTION REQ'D
DIMENSIONS MARKED ◆ —— TOTAL ——
UNLESS OTHERWISE STATED
1. DIMENSIONS ARE IN INCHES
2. TOLERANCES ARE
± 0.06 FOR ONE DECIMAL
± 0.03 FOR TWO DECIMALS
± 0.01 FOR THREE DECIMALS
± 1° FOR ANGLES

PROJ. ENG.	A.P.W.	3/19/81
CH. OF DES.		
DES. SUP.		
DRAFTSMAN		
CK. BY	R. BOSSE	3/19/81

ENGINEER
WORK SHEET
PARTS LIST
ITEM | ZONE
NO REQ'D
SCALE

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UNITED TECHNOLOGIES RESEARCH CENTER
East Hartford, Connecticut 06108

FOSS RECEIVER

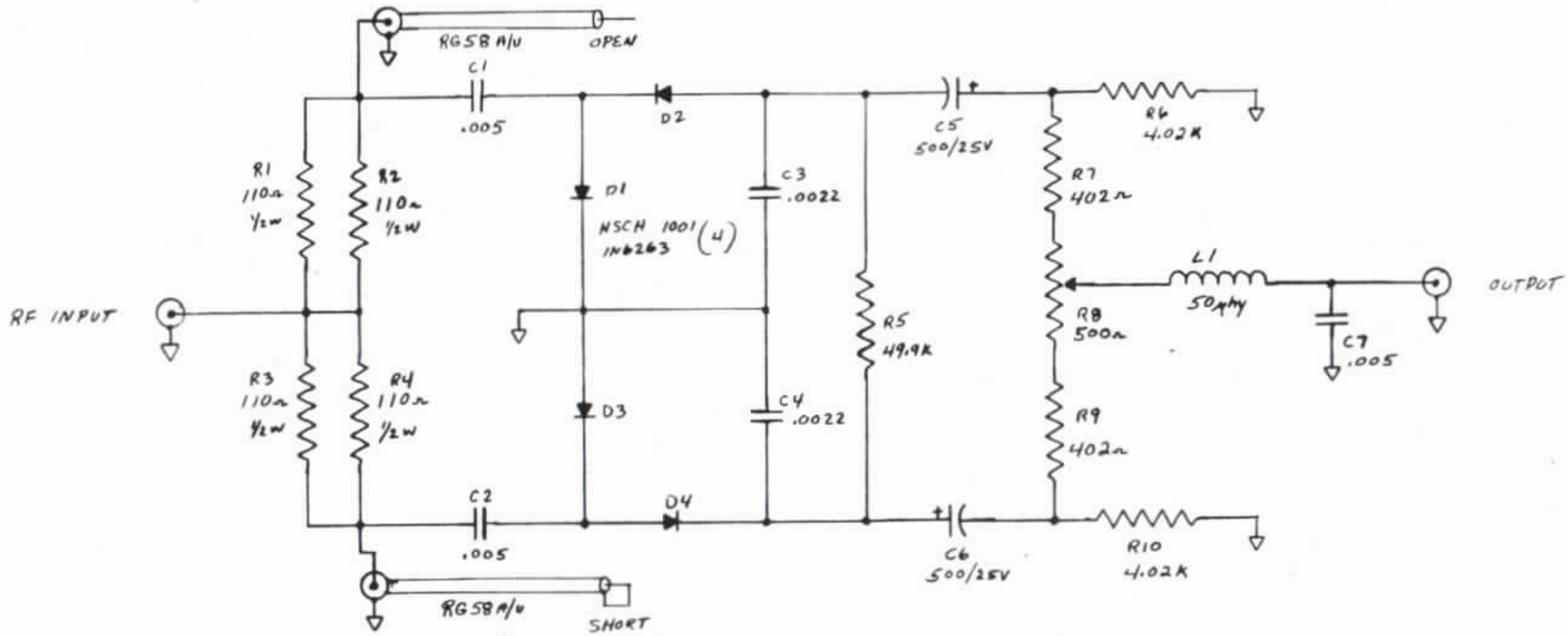
COUNT DOWN CKT

(PART OF FREQUENCY SYNTHESIZER)

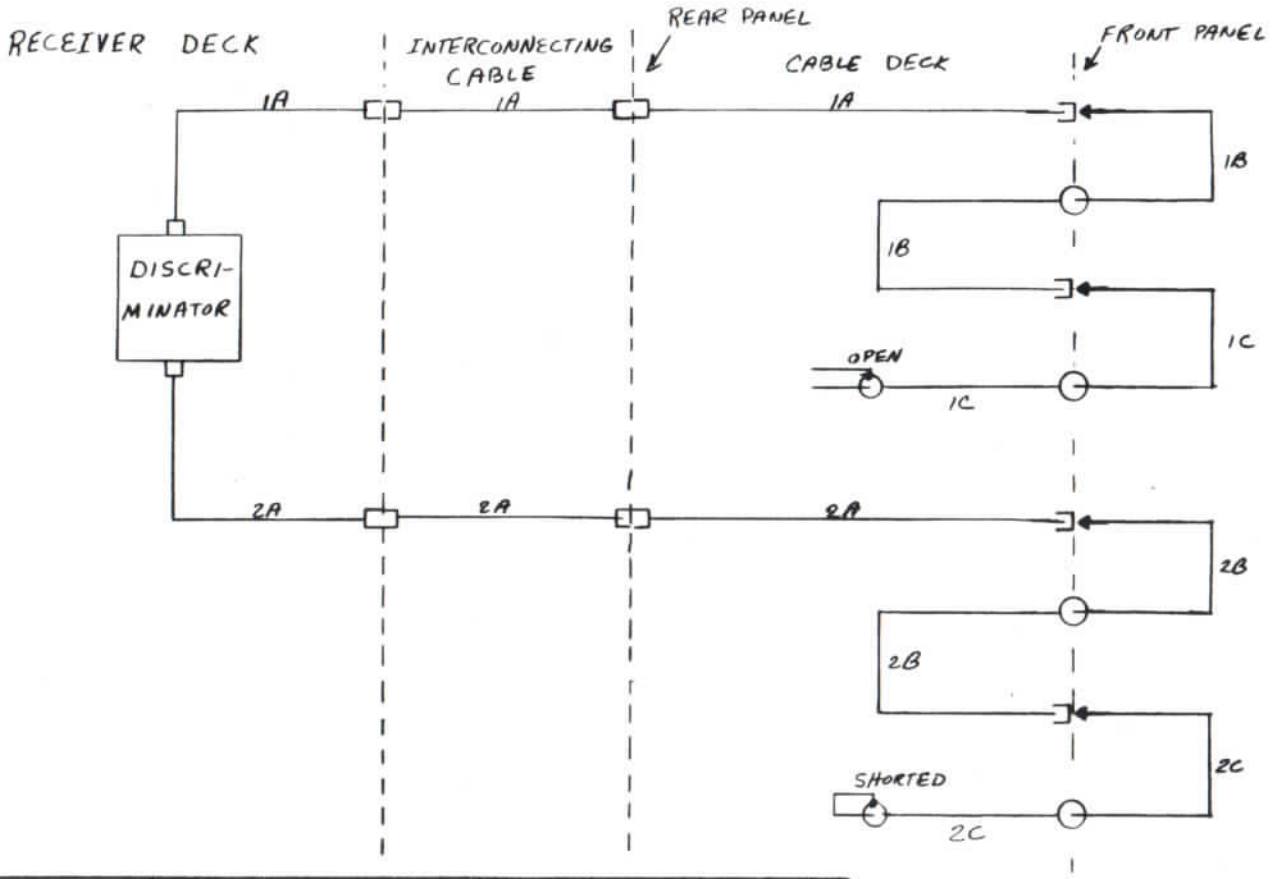
PROJ NO. : ESG 634-1-6

NEXT ASS'Y

REV.

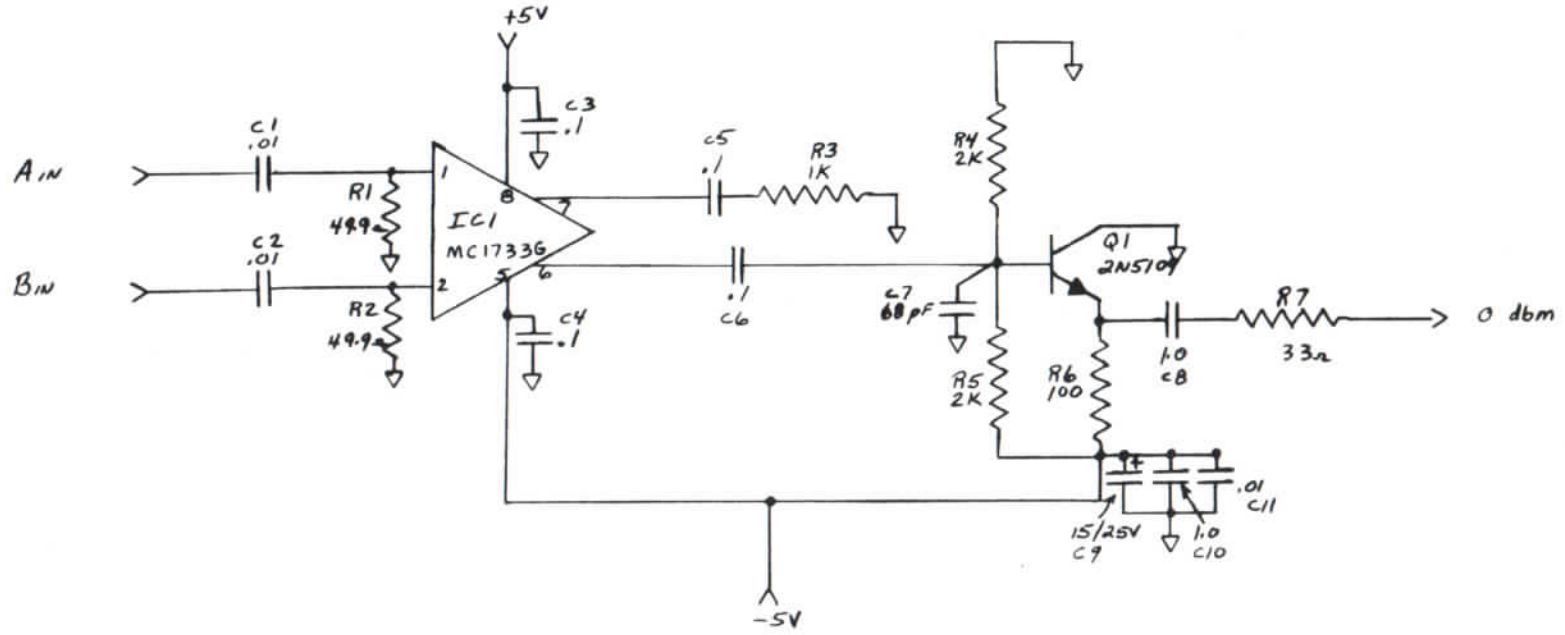


INSPECTION REQ'D DIMENSIONS MARKED ● —— TOTAL ——	ENGINEER	DISCRIMINATOR SCHEMATIC -FOSS- (PART OF RECEIVER)	REV.	BY	DATE	APP.	DWG. NO. ESG634-1-7
UNLESS OTHERWISE STATED 1. DIMENSIONS ARE IN INCHES 2. TOLERANCES ARE ± 0.06 FOR ONE DECIMAL ± 0.03 FOR TWO DECIMALS ± 0.01 FOR THREE DECIMALS ± 1° FOR ANGLES	WORK SHEET / PARTS LIST						
	ITEM / ZONE	MAT'L					
PROJ. ENG.	NO. REQ'D	NEXT ASS'Y	PROJ. NO. 925265				
CH. OF DES.							
DES. SUP.							
DESIGNER	SCALE	UNITED TECHNOLOGIES RESEARCH CENTER East Hartford, Connecticut 06108					REV
CHK. BY							
DRAWN BY R. BOSSE 3/9/81							



INSPECTION REQ'D DIMENSIONS MARKED ● —— TOTAL ——			ENGINEER	TIMING CABLE CHASSIS - FOSS -	REV.	BY	DATE	APP.
UNLESS OTHERWISE STATED 1. DIMENSIONS ARE IN INCHES 2. TOLERANCES ARE ± 0.06 FOR ONE DECIMAL, ± 0.03 FOR TWO DECIMALS ± 0.01 FOR THREE DECIMALS ± 1° FOR ANGLES			WORK SHEET					
			PARTS LIST					
			ITEM	ZONE	MAT'L			
					NEXT ASS'Y	PROJ. NO.		
PROJ. ENG.	AHV	5/3/91	NO. REQ'D		PROPRIETARY NOTICE: THIS DOCUMENT is the property of United Technologies Corporation and is delivered on the express condition that it is not to be disclosed, reproduced in whole or in part, or used for manufacture for anyone other than United Technologies Corporation without its written consent, and that no right is granted to disclose or so use any information contained in said document. This restriction does not limit the right to use information obtained from another source.			
CH. OF DEE.								
DEE. SUP.								
DESIGNER			SCALE		UNITED TECHNOLOGIES RESEARCH CENTER East Hartford, Connecticut 06108			
CHK. BY								
DRAWN BY	R. Bossi	5/15/91						

DWG. NO. ESG 634-1-8 REV.



INSPECTION REQ'D DIMENSIONS MARKED ● ——— TOTAL ———	ENGINEER	DIFFERENTIAL PREAMP -FOSS-	REV.	BY	DATE	APP.	DWG NO. E56 634-1-9
UNLESS OTHERWISE STATED 1. DIMENSIONS ARE IN INCHES 2. TOLERANCES ARE ± 0.06 FOR ONE DECIMAL ± 0.03 FOR TWO DECIMALS ± 0.01 FOR THREE DECIMALS ± 1° FOR ANGLES	WORK SHEET						
	PARTS LIST						
	ITEM / ZONE	MAT'L					
PROJ. ENG. A. Hill 5/15/81	NO. REQ'D	NEXT ASS'Y	PROJ. NO.				
CH. OF DES.		PROPRIETARY NOTICE: This document is the property of United Technologies Corporation and is delivered on the express condition that it is not to be disclosed, reproduced in whole or in part, or used for manufacture for anyone other than United Technologies Corporation without its written consent, and that no right is granted to disclose or so use any information contained in said document. This restriction does not limit the right to use information obtained from another source.					
DES. SUP.							
DESIGNER	SCALE	UNITED TECHNOLOGIES RESEARCH CENTER East Hartford Connecticut 06108					REV. A
CHK. BY							
DRAWN BY R. Boss 5/15/81							